

REMARKS

Favorable reconsideration of this application in view of the following remarks is respectfully requested.

Claims 14-19 are presented for examination on this application. Claims 1-13 have been previously cancelled without prejudice or disclaimer. Claim 14 has been amended to clarify that the gate electrode is a conductive layer as fully supported at page 16, lines 2-8, for example so that there has been no introduction of any new matter. Claim 19 has been further added to even more clearly define the overlap of the edges of gate electrode conductive layer and the opposing edges of the first impurity diffusion layer and the second impurity diffusion layer as shown by FIG. 16, for example.

The outstanding Action presented a rejection of Claims 14-18 under 35 U.S.C. §102(b) as being anticipated by admitted prior art as illustrated in Application Figures 1-8.

Initially, the Examiner is thanked for the clarification presented in the telephone conversation of March 1, 2004, that the above noted rejection is predicated upon reading the "gate electrode" of FIG. 8 as being a gate structure that would include the gate insulating film under the conductive gate portion that protrudes past the side edges of the conductive gate portion to overlap the first and second impurity diffusion layers.

A first possible modification to Claim 14 was discussed in terms of deleting the "overlapped relation" language of Claim 14 and substituting language requiring that an edge of the gate electrode is disposed immediately above the edge of at least one of the first and second impurity diffusion layers. The Examiner indicated that this change would not be effective as the reading of the gate electrode as the gate structure including the gate insulating film under the

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conductive gate portion that protrudes past the side edges of the conductive gate portion would be readable as disposed immediately above edges of the first and second impurity diffusion layers.

A change to the recitation of the gate electrode was also discussed in terms of reciting that the gate electrode was formed as a conductive layer in the trench with the gate insulting film intervening between the gate electrode conductive layer and the trench. The Examiner acknowledged that FIG. 8 did not show such a gate electrode conductive layer being formed in an overlapped relation relative to the first impurity diffusion layer and the second impurity diffusion layer and indicated that such a limitation should overcome the above-noted rejection.

Accordingly, as Claim 14 has been amended to require the gate electrode to be formed as a conductive layer and that this gate electrode conductive layer must be in an overlapped relation relative to the first impurity diffusion layer and the second impurity diffusion layer.

Thus, it is believed that the rejection of Claims 14-18 under 35 U.S.C. §102(b) as being anticipated by admitted prior art as illustrated in Application Figures 1-8 has been overcome and that this rejection should, therefore, be withdrawn.

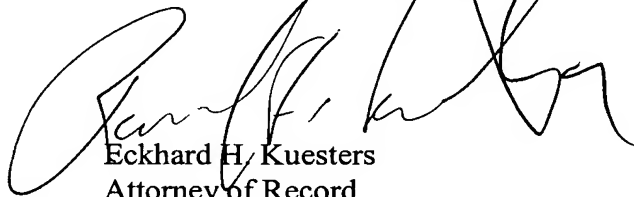
Moreover, as new Claim 19 also recites the gate electrode to be formed as a conductive layer and that this gate electrode conductive layer must have both side edges disposed immediately above opposing edges of the first impurity diffusion layer and the second impurity diffusion layer, it is believed that Claim 19 also patentably defines over the showings of Figures 1-8.

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Accordingly, as no further issues are believed to remain outstanding in the present application, it is believed that this application is clearly in condition for formal allowance and an early and favorable action to this effect is earnestly and respectfully requested.

Respectfully submitted,

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A handwritten signature in black ink, appearing to read 'Eckhard H. Kuesters', is written over the printed name and title.

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